1. Problem Statement: 8-bit BCD Adder

Design code

module bcd\_adder(

input [7:0] A,

input [7:0] B,

input Cin,

output [7:0] S,

output Cout

);

logic [3:0] lsum, hsum;

logic lcarry, hcarry;

assign {lcarry, lsum} = A[3:0] + B[3:0] + Cin;

assign {hcarry, hsum} = A[7:4] + B[7:4] + (lsum > 4'd9);

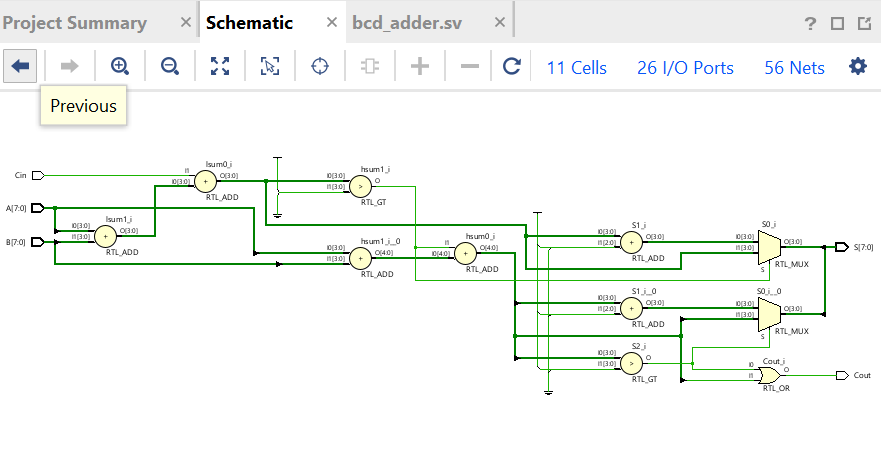
assign S = { (hsum > 4'd9) ? (hsum + 4'd6) : hsum,

(lsum > 4'd9) ? (lsum + 4'd6) : lsum };

assign Cout = (hsum > 4'd9) || hcarry;

endmodule

RTL



Testbenh:

module testbench;

reg [7:0] A;

reg [7:0] B;

reg Cin;

wire [7:0] S;

wire Cout;

bcd\_adder uut (

.A(A),

.B(B),

.Cin(Cin),

.S(S),

.Cout(Cout)

);

initial begin

$monitor("Time: %0d | A=%d B=%d Cin=%b | S=%d Cout=%b", $time, A, B, Cin, S, Cout);

A = 8'd45; B = 8'd36; Cin = 0; #10;

A = 8'd99; B = 8'd99; Cin = 0; #10;

A = 8'd12; B = 8'd89; Cin = 1; #10;

A = 8'd50; B = 8'd50; Cin = 0; #10;

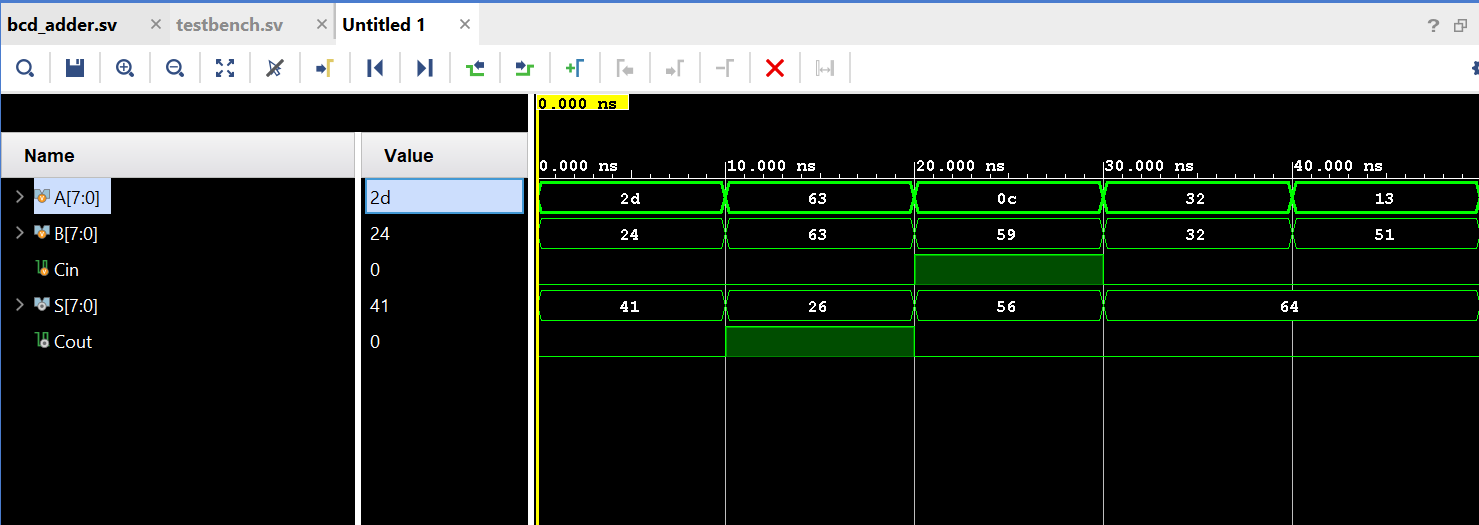
A = 8'd19; B = 8'd81; Cin = 0; #10;

$finish;

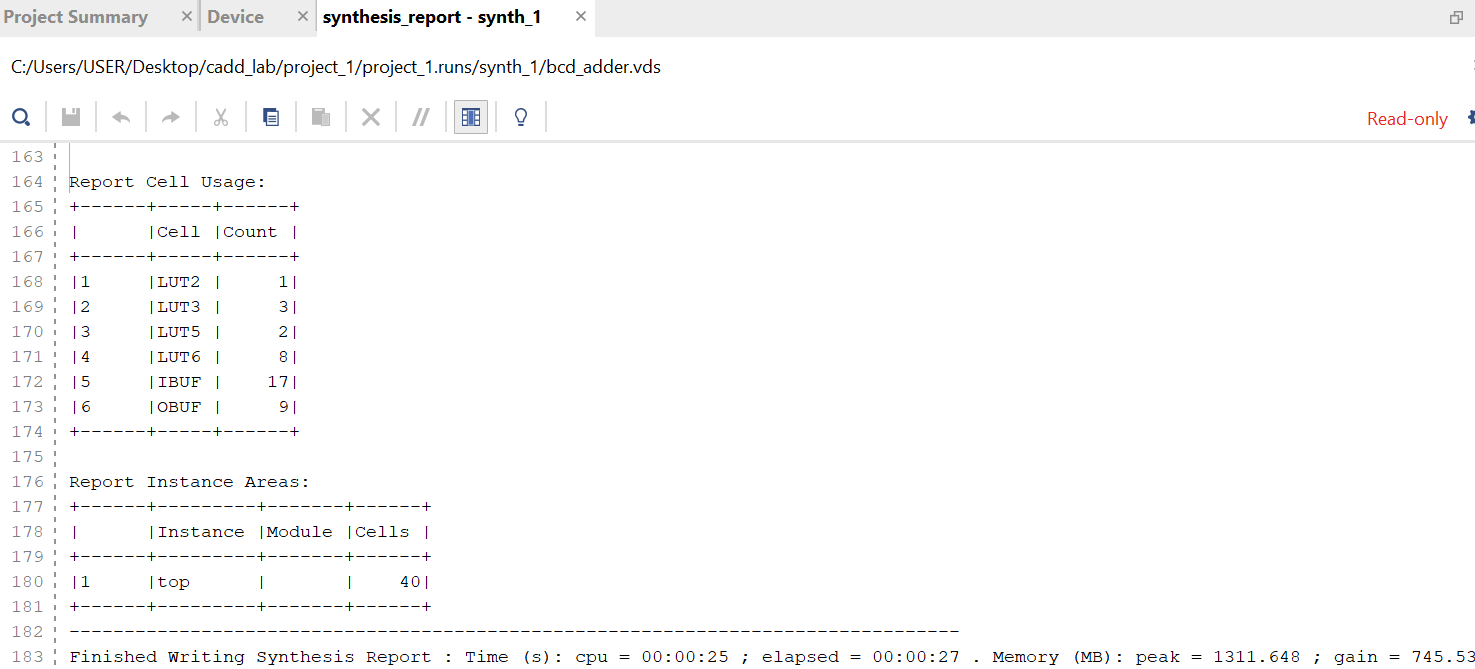
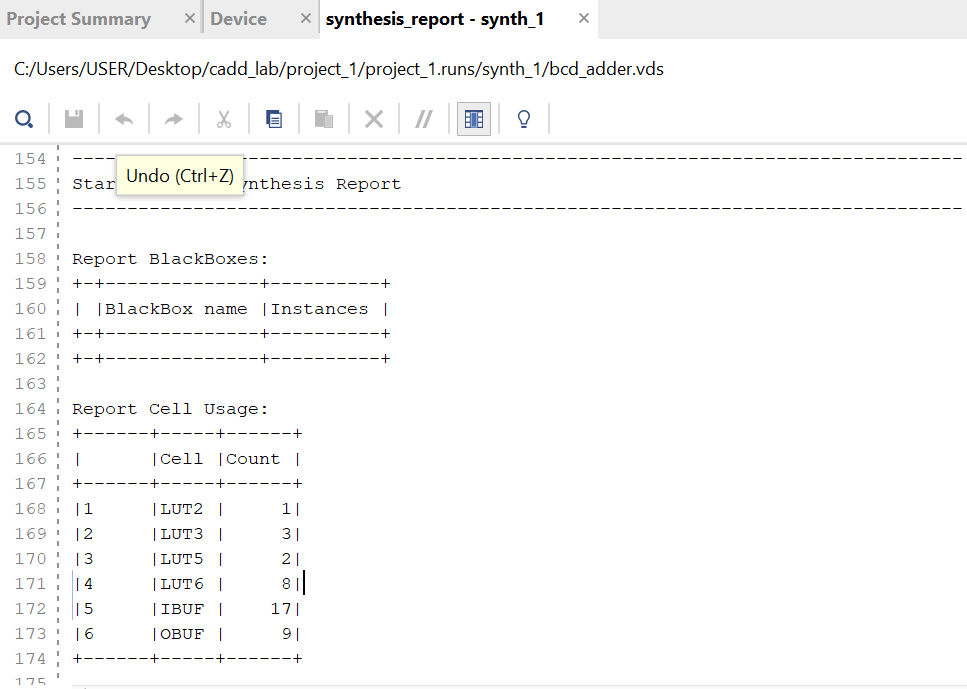
end

endmodule

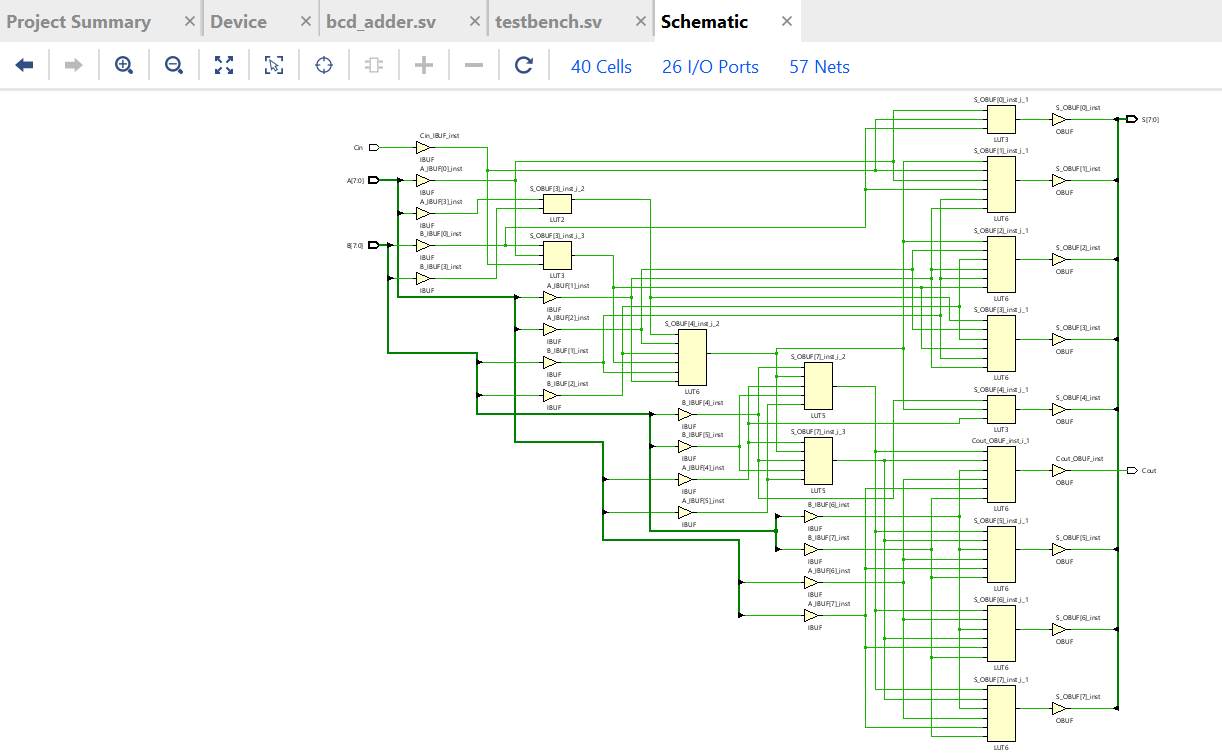
wave form:



Synthesis reort:



TECHNOLOGY DIAGRAM



2.Problem Statement: FPGA Flow – Combinational & Sequential circuits

**(a) Boolean Simplification**

Design code:

module combinational\_a (

input A, B, C, D,

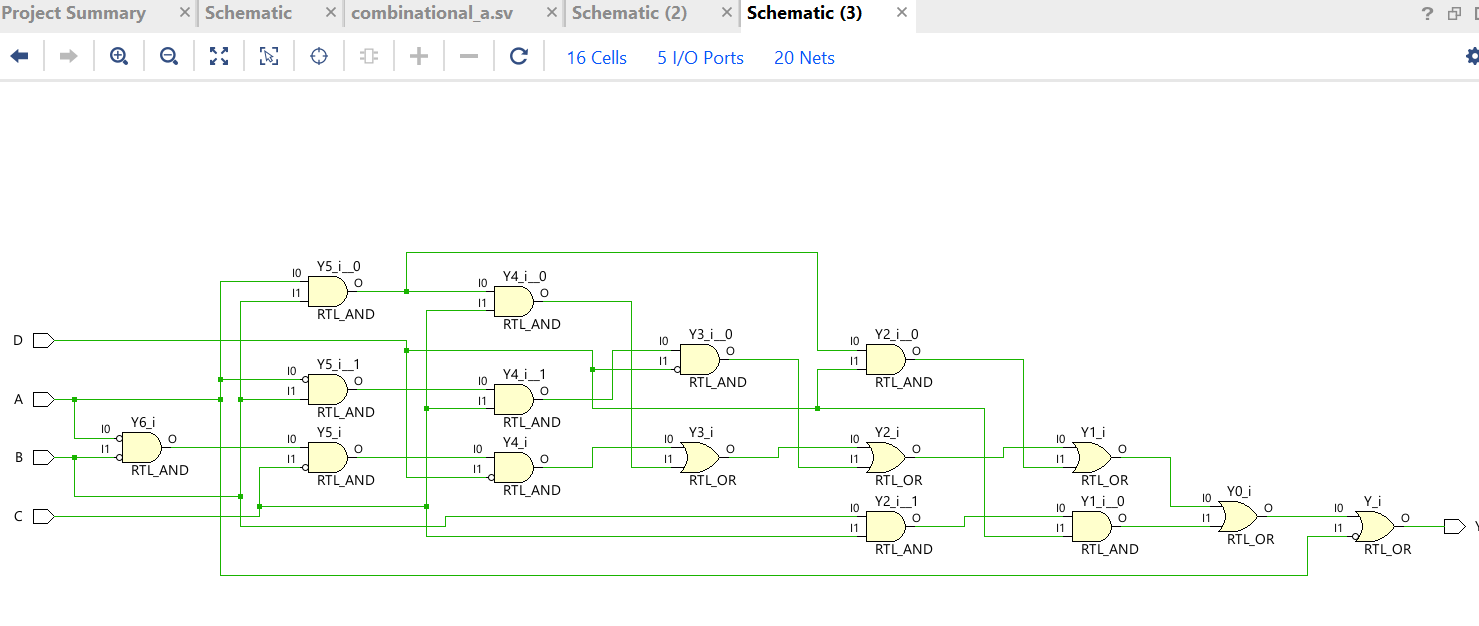
output Y

);

assign Y = (~A & ~B & ~C & ~D) | (A & B & C) | (~A & B & C & ~D) | (A & B & D) | (B & C & D) | (~A);

endmodule

RTL:



**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

TESTBENCH:

module testbench;

logic A, B, C, D;

logic Y;

combinational\_a uut (

.A(A), .B(B), .C(C), .D(D), .Y(Y) );

initial begin

$display("Testbench for comb\_function1");

$display("A B C D | Y");

A = 0; B = 0; C = 0; D = 0; #5;

$display("%b %b %b %b | %b", A, B, C, D, Y);

A = 1; B = 0; C = 1; D = 1; #5;

$display("%b %b %b %b | %b", A, B, C, D, Y);

A = 1; B = 1; C = 0; D = 1; #5;

$display("%b %b %b %b | %b", A, B, C, D, Y);

A = 0; B = 1; C = 1; D = 0; #5;

$display("%b %b %b %b | %b", A, B, C, D, Y);

A = 1; B = 1; C = 1; D = 1; #5;

$display("%b %b %b %b | %b", A, B, C, D, Y);

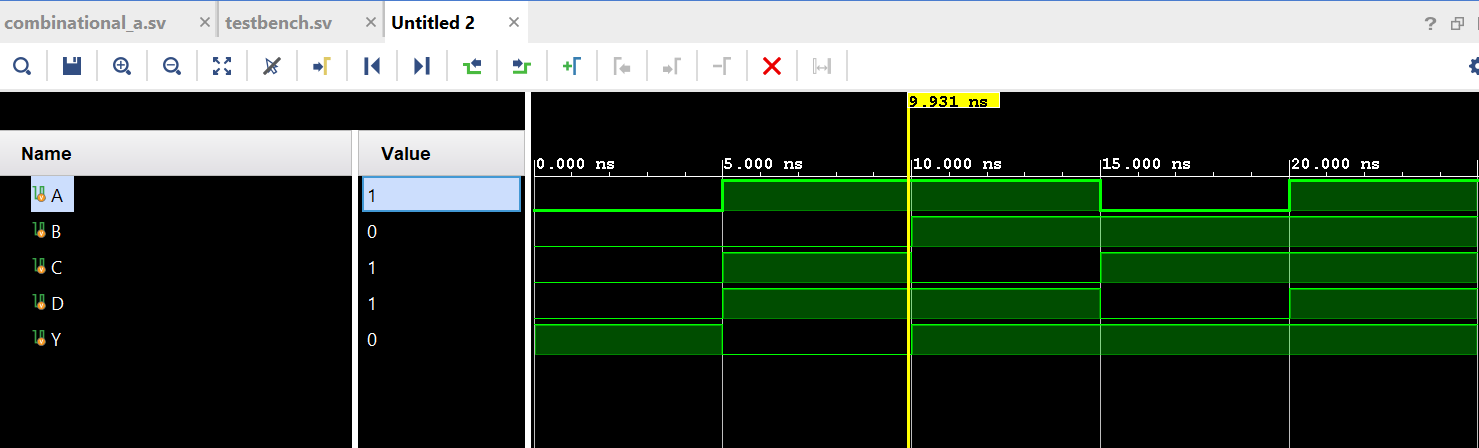
$display("Test complete.");

$finish;

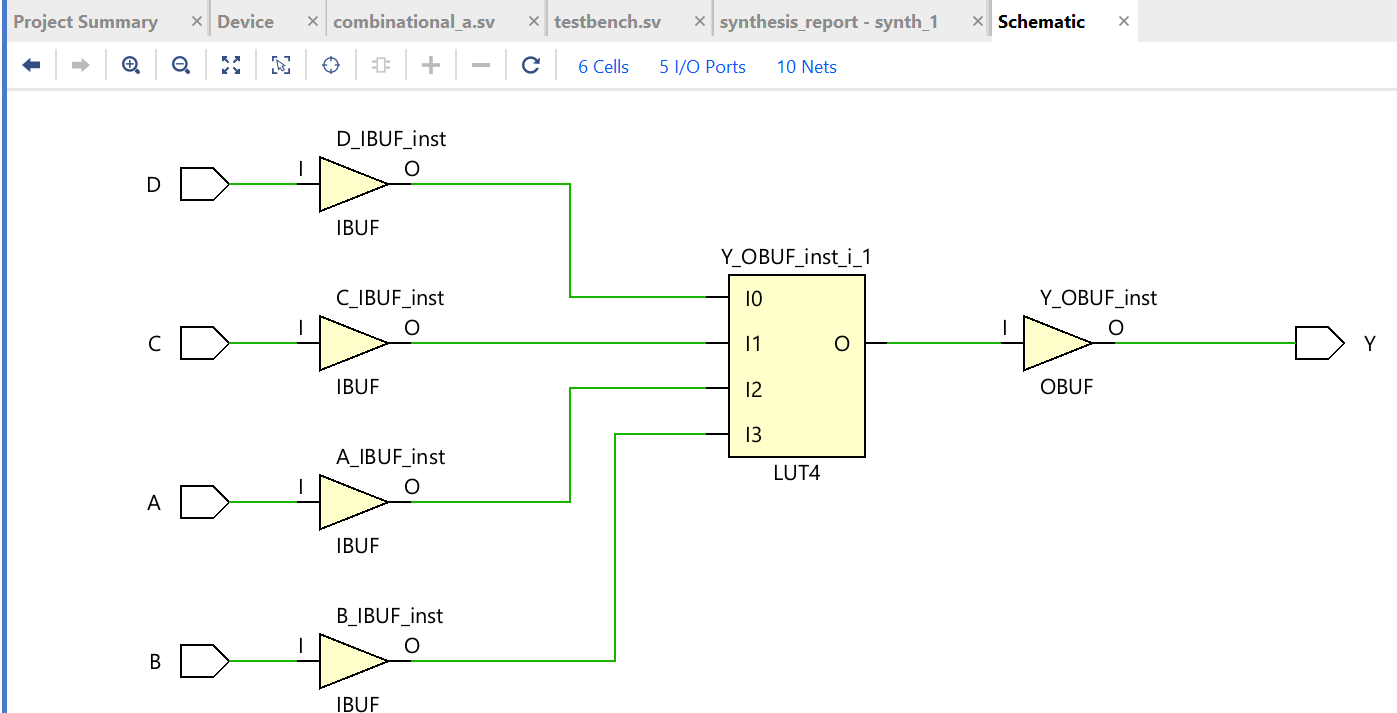
end

endmodule

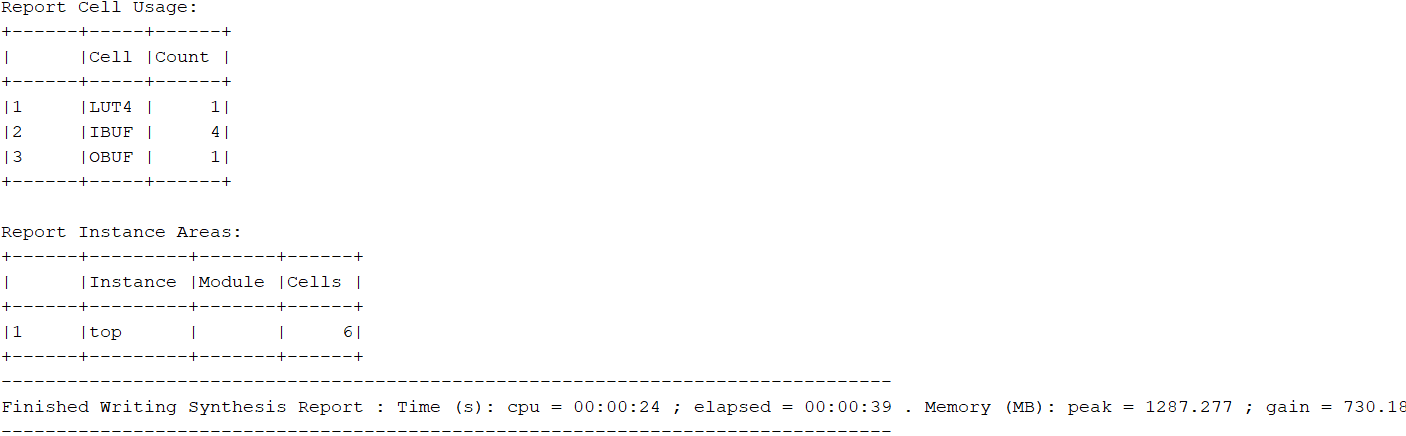
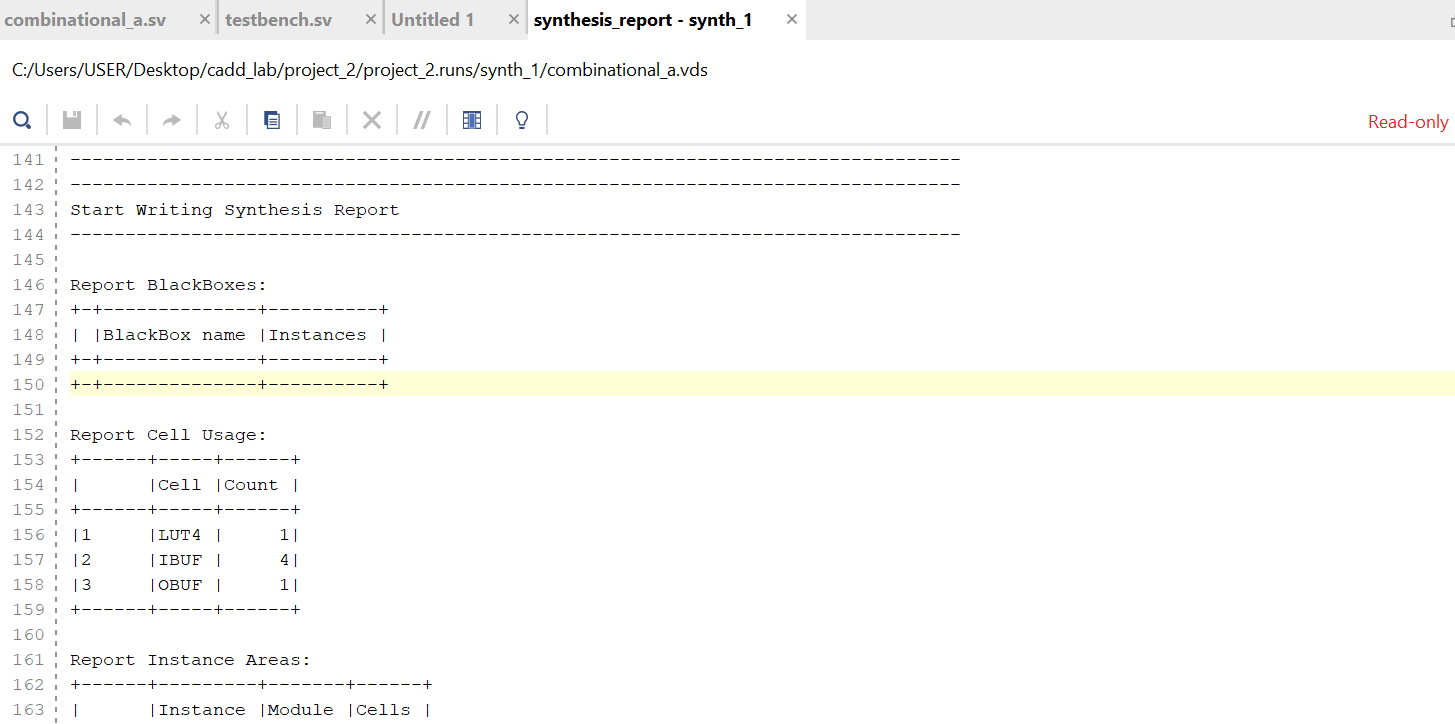
WAVEFORM:



TECHNOLOGY SCREENSHOT:



Synthesis REPORT:



**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**(b)COMBINATIONAL\_B**

**DESIGN CODE:**

**module combinational\_b (**

**input A, B, C, D, E,**

**output Y**

**);**

**assign Y = (A & B & C) | (A & B & D) | (A & B & E) | (A & C & D) | (A & C & E) |**

**(A | D | E) | (B & C & D) | (B & C & E) | (B & D & E) | (C & D & E);**

**Endmodule**

**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**Testbench**

**module testbench;**

**logic A, B, C, D, E;**

**logic Y;**

**combinational\_b uut (**

**.A(A), .B(B), .C(C), .D(D), .E(E), .Y(Y) );**

**initial begin**

**$display("Testbench for comb\_function2");**

**$display("A B C D E | Y");**

**// Test cases**

**A = 0; B = 0; C = 0; D = 0; E = 0; #5; $display("%b %b %b %b %b | %b", A, B, C, D, E, Y);**

**A = 1; B = 0; C = 1; D = 1; E = 0; #5; $display("%b %b %b %b %b | %b", A, B, C, D, E, Y);**

**A = 0; B = 1; C = 0; D = 1; E = 1; #5; $display("%b %b %b %b %b | %b", A, B, C, D, E, Y);**

**A = 1; B = 1; C = 1; D = 0; E = 1; #5; $display("%b %b %b %b %b | %b", A, B, C, D, E, Y);**

**A = 1; B = 1; C = 1; D = 1; E = 1; #5; $display("%b %b %b %b %b | %b", A, B, C, D, E, Y);**

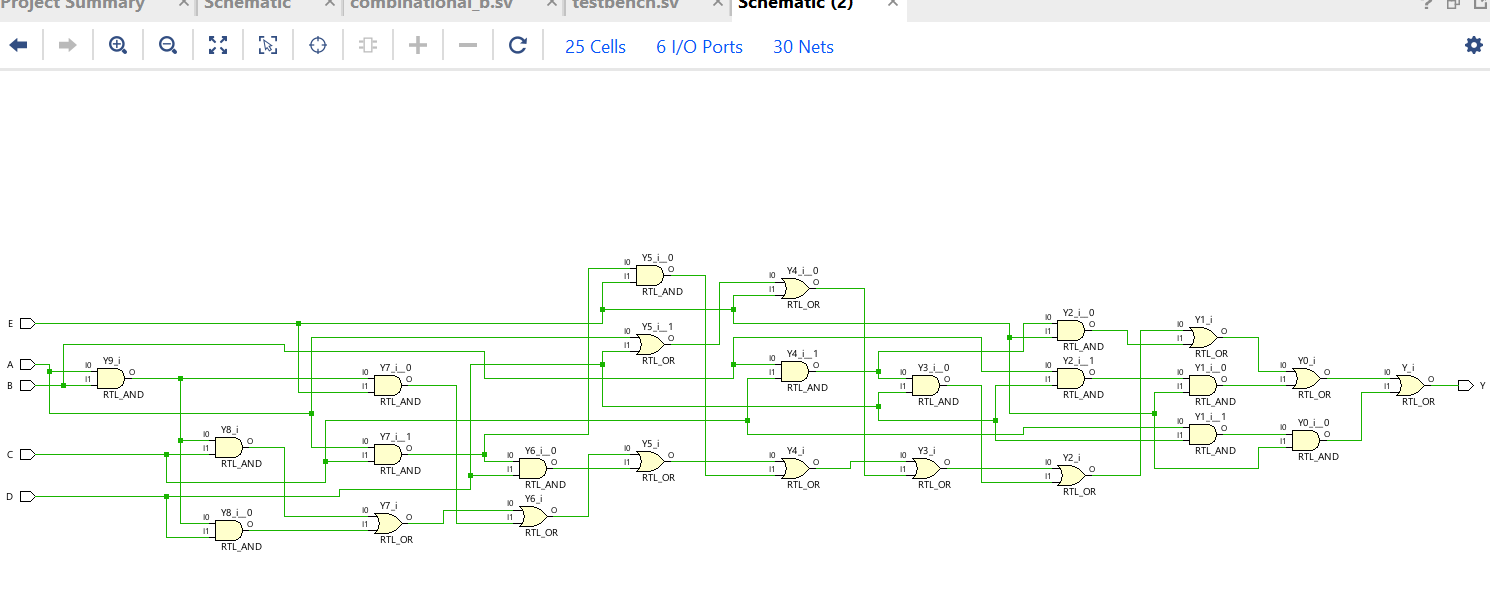
**$display("Test complete.");**

**$finish;**

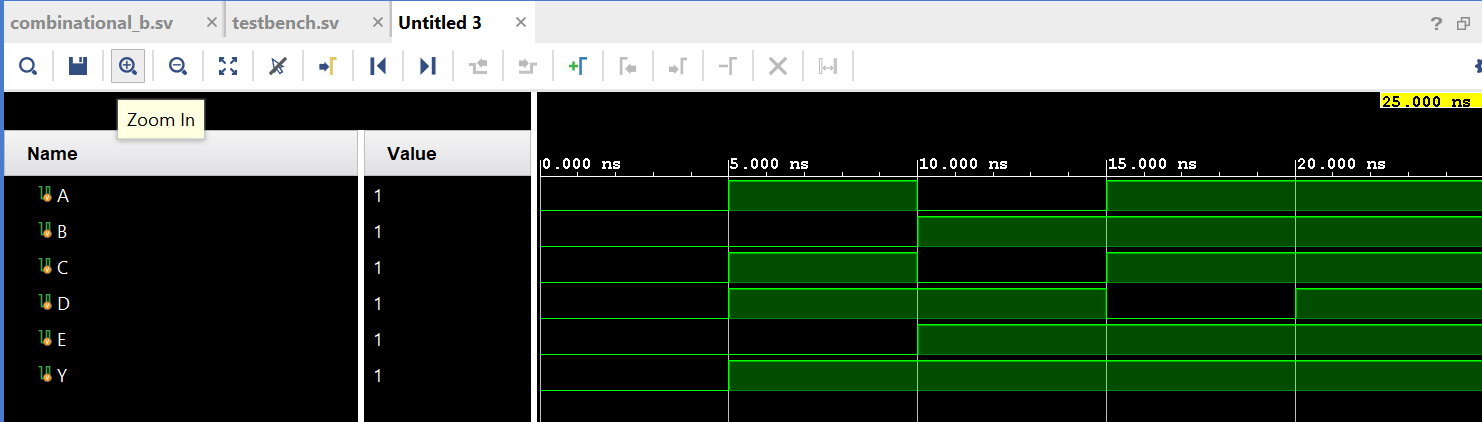
**end**

**endmodule**

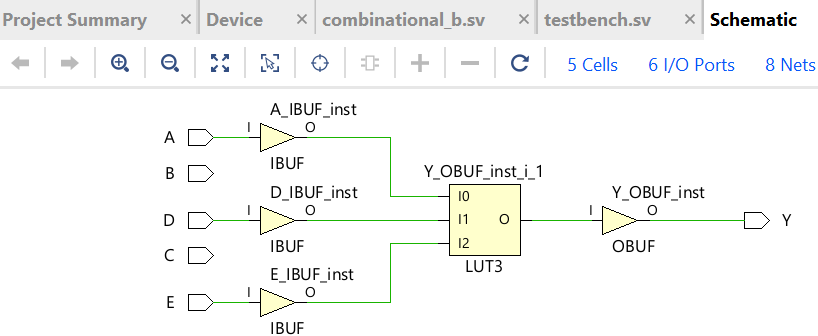
**RTL:**

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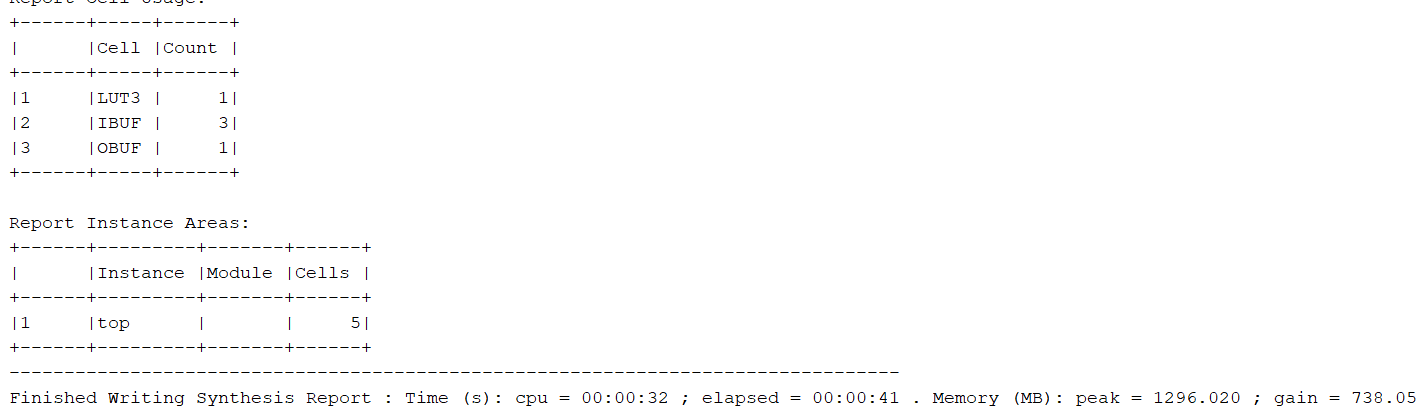
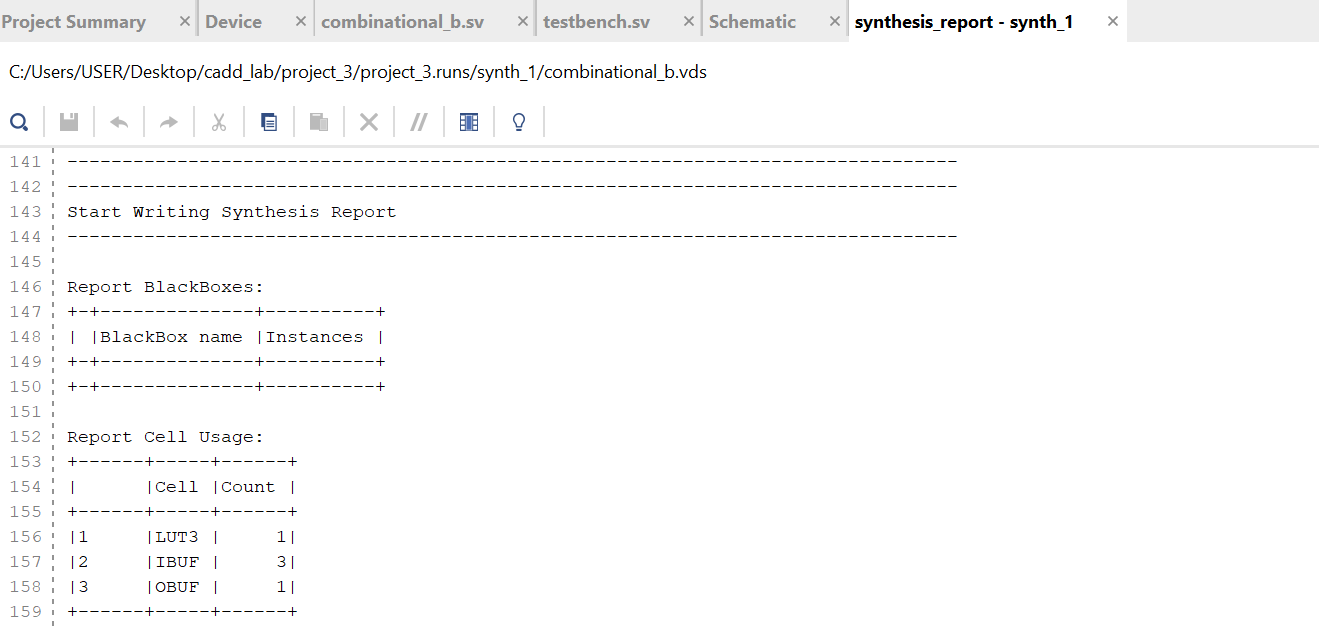
**WAVEFORM:**

****

TECNOLOGY SCREENSHOT:



SYNTHESIS REPORT:



**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

(c): **Two-Output Function**

**DESIGN CODE:**

module two\_output\_function(input A, B, C, D, output Y1, Y2);

assign Y1 = A | (B & C) | ~D;

assign Y2 = A & B & ~C & D;

endmodule

TESTBENCH:

module testbench;

reg A, B, C, D;

wire Y1, Y2;

two\_output\_function uut (.A(A), .B(B), .C(C), .D(D), .Y1(Y1), .Y2(Y2));

initial begin

$monitor("A=%b, B=%b, C=%b, D=%b -> Y1=%b, Y2=%b", A, B, C, D, Y1, Y2);

A = 0; B = 0; C = 0; D = 0;

#10;

A = 1; B = 0; C = 1; D = 0;

#10;

A = 0; B = 1; C = 0; D = 1;

#10;

A = 1; B = 1; C = 1; D = 1;

#10;

A = 0; B = 1; C = 1; D = 0;

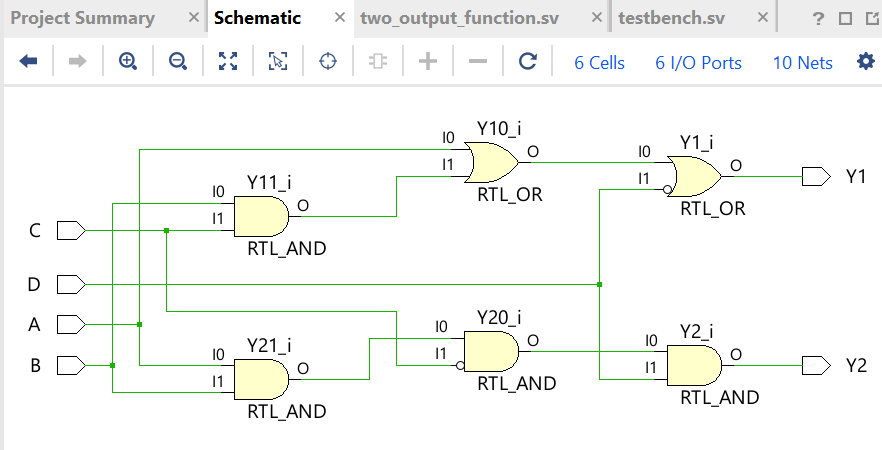
#10;

$finish;

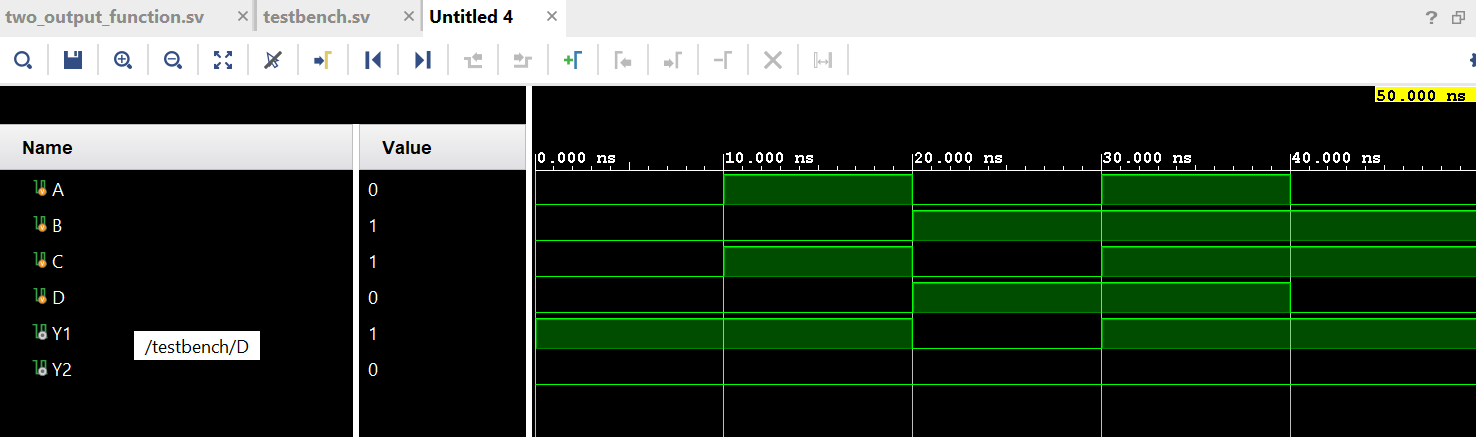
end

endmodule

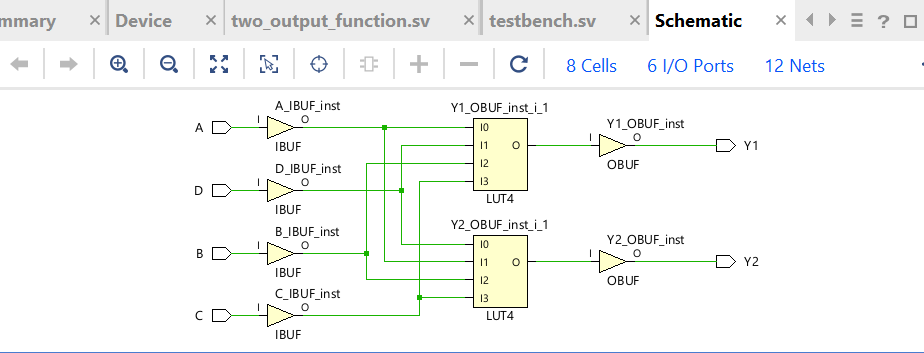
RTL:



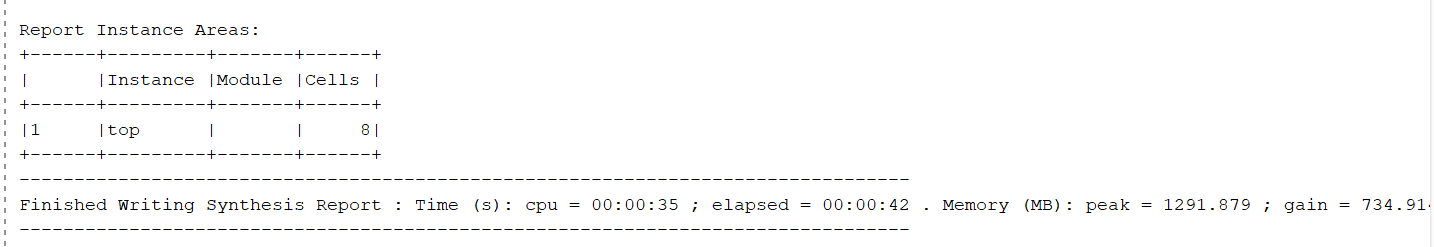
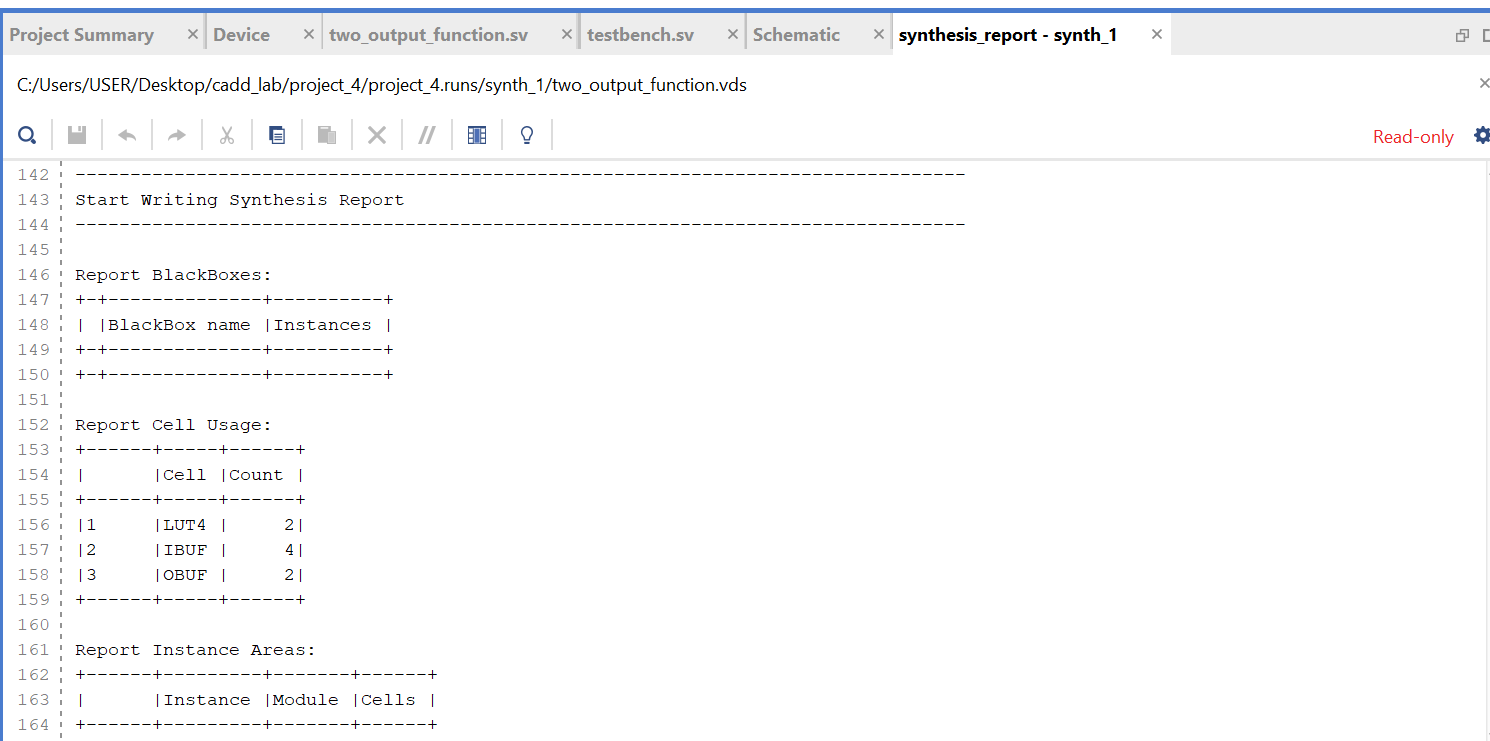
WAVEFORM;



TECHNOLOGY SCREENSHOT:



SYMTHESIS REPORT:



**\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

**(d) Prime Number and Divisibility Logic**

**Design Code :**

**module divisibility(input [3:0] A, output P, D);**

**assign P = (A == 4'd2) | (A == 4'd3) | (A == 4'd5) |**

**(A == 4'd7) | (A == 4'd11) | (A == 4'd13);**

**assign D = (A % 3 == 0);**

**endmodule**

**TESTBENCH:**

**module testbench;**

**reg [3:0] A;**

**wire P, D;**

**divisibility uut (.A(A), .P(P), .D(D));**

**initial begin**

**$monitor("A=%b (%d) -> P=%b (Prime), D=%b (Divisible by 3)", A, A, P, D);**

**A = 4'd0; #10;**

**A = 4'd3; #10;**

**A = 4'd5; #10;**

**A = 4'd9; #10;**

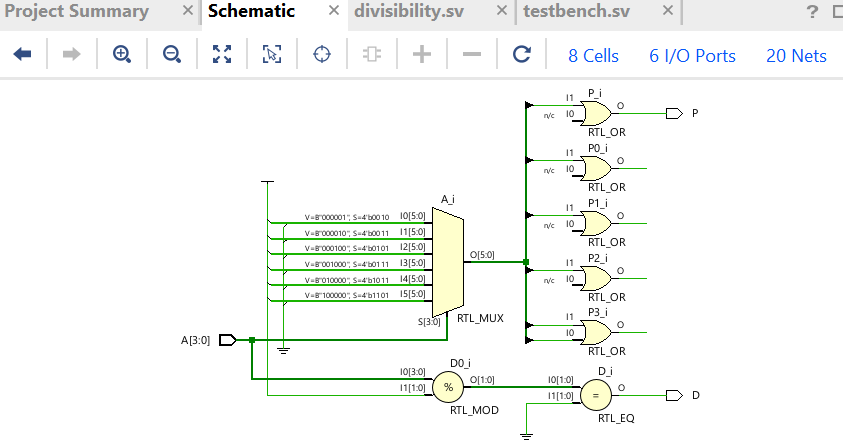
**A = 4'd14; #10;**

**$finish;**

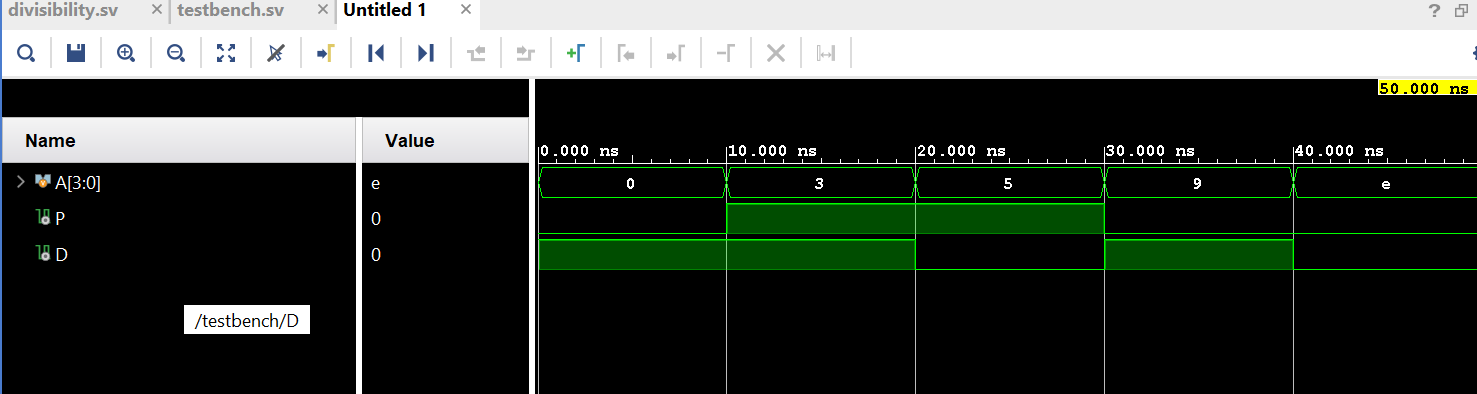
**end**

**endmodule**

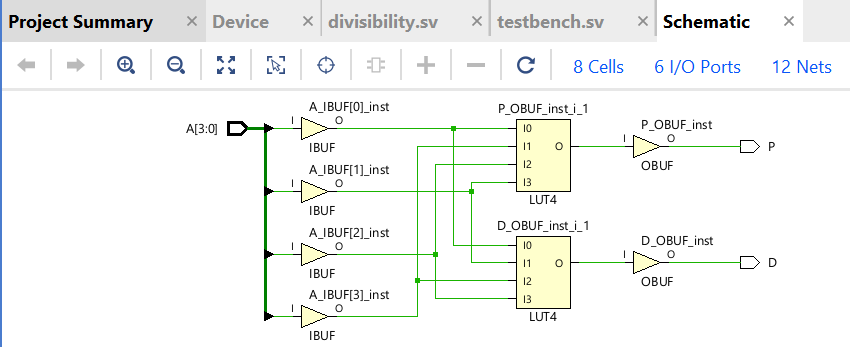
RTL:

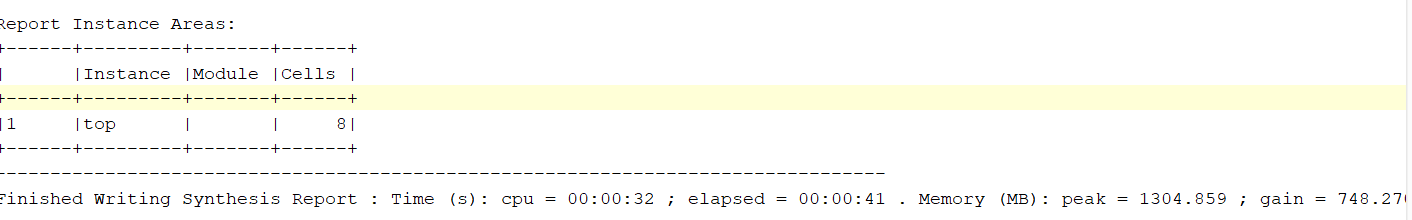
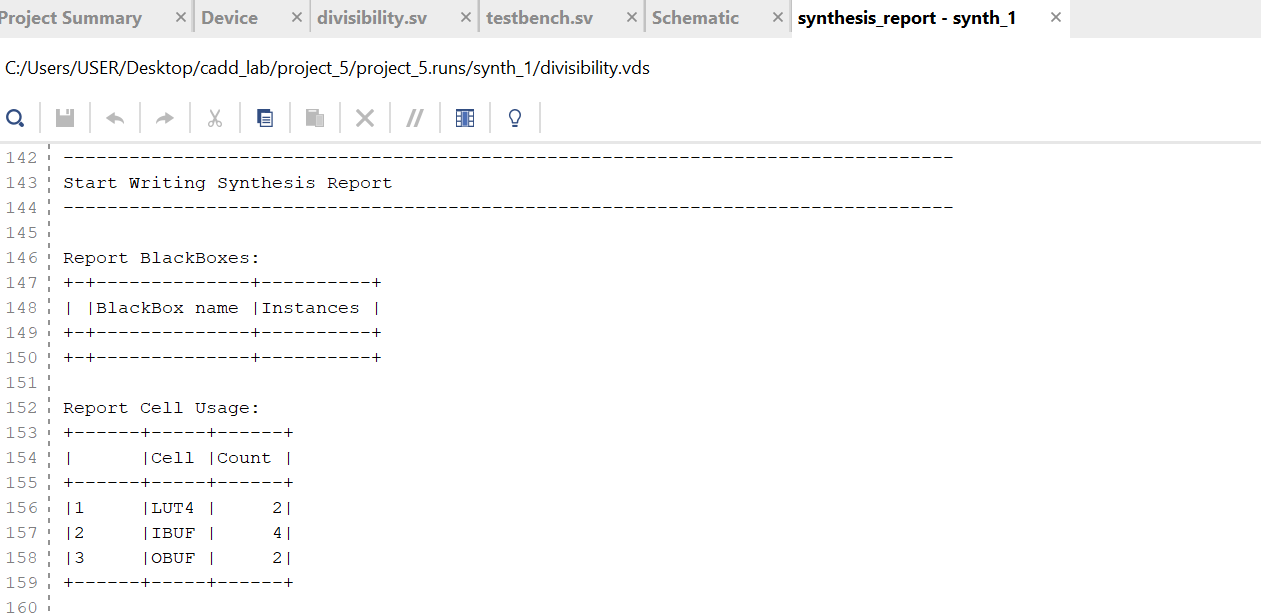


WAVEFORM:



TECNOLOGY SCREENSHOT:

SYNTHESIS REPORT:



(e): 4-Bit Priority Encoder

DESIGN CODE:

module priority\_encoder\_4(input [3:0] A, output logic [1:0] Y, output reg valid);

always @(\*) begin

valid = (A != 0);

casez (A)

4'b1???: Y = 2'b11;

4'b01??: Y = 2'b10;

4'b001?: Y = 2'b01;

4'b0001: Y = 2'b00;

default: Y = 2'b00;

endcase

end

endmodule

TESTBENCH

module testbench;

reg [3:0] A;

wire [1:0] Y;

wire valid;

priority\_encoder\_4 uut (.A(A), .Y(Y), .valid(valid));

initial begin

$monitor("A=%b -> Y=%b, Valid=%b", A, Y, valid);

A = 4'b0000; #10;

A = 4'b0001; #10;

A = 4'b1000; #10;

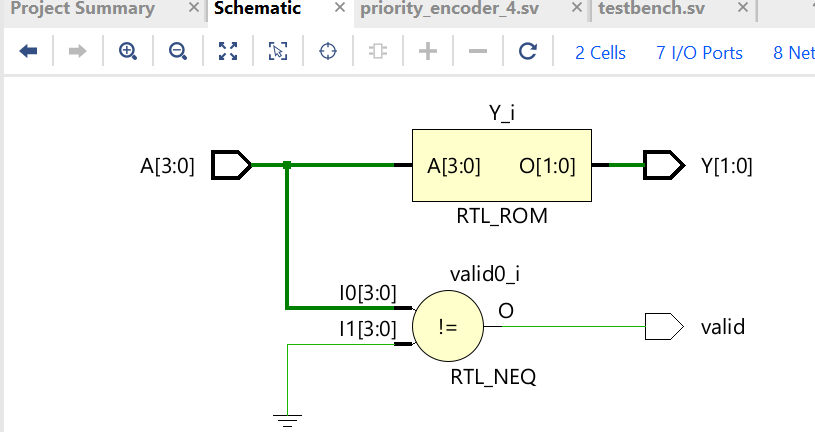
A = 4'b1010; #10;

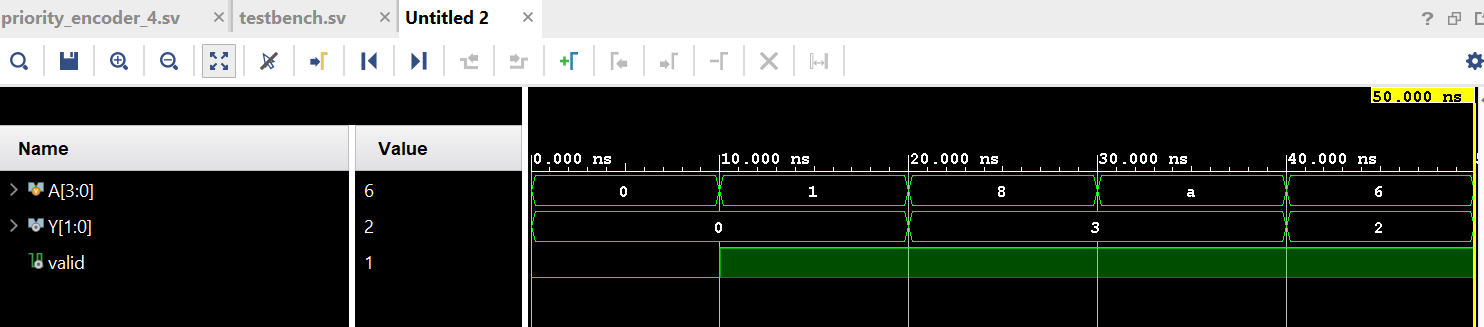
A = 4'b0110; #10;

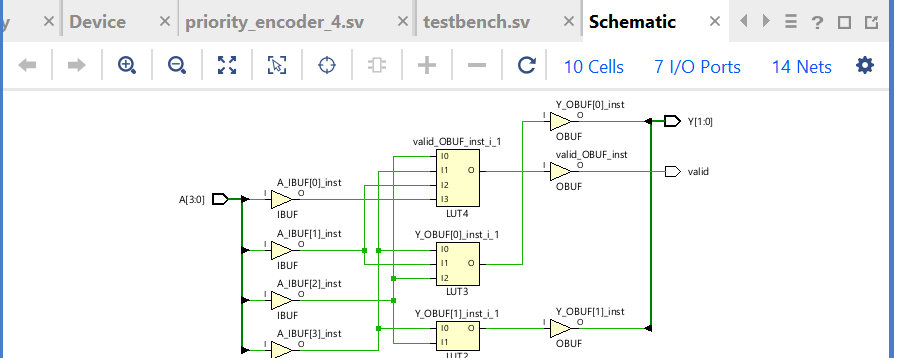
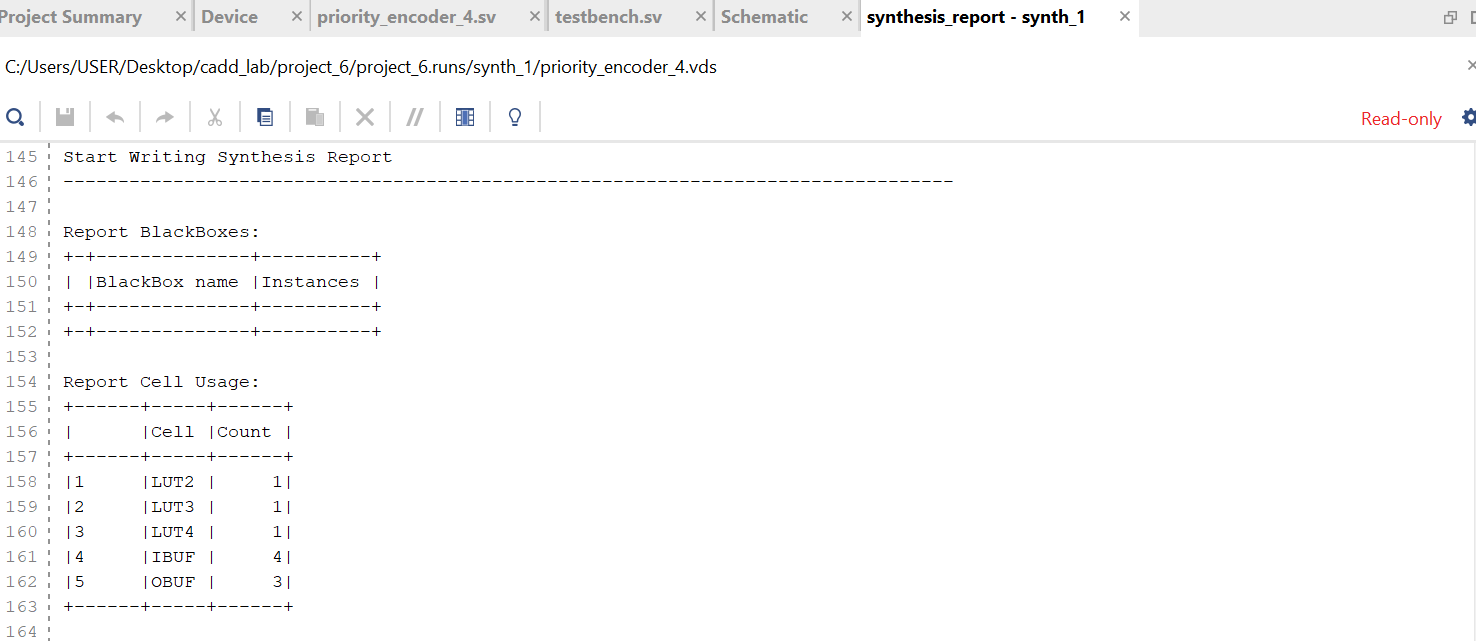
$finish;

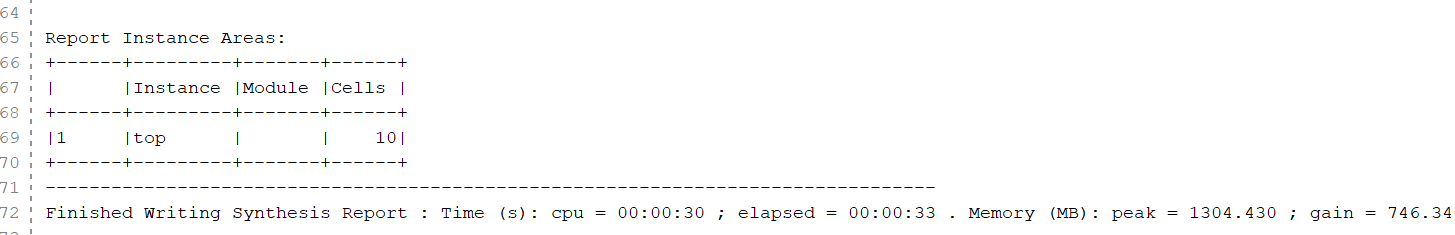
end

endmodule

RTL: WAVEFORM:

TECHNOLOGY SCREENSHOT:

SYNTHESIS REPORT: 



(f) 8-Bit Priority Encode

module priority\_encoder\_8(input [7:0] A, output logic [2:0] Y, output reg valid);

always @(\*) begin

valid = (A != 0);

casez (A)

8'b1???????: Y = 3'b111;

8'b01??????: Y = 3'b110;

8'b001?????: Y = 3'b101;

8'b0001????: Y = 3'b100;

8'b00001???: Y = 3'b011;

8'b000001??: Y = 3'b010;

8'b0000001?: Y = 3'b001;

8'b00000001: Y = 3'b000;

default: Y = 3'b000;

endcase

end

endmodule

TESTBENCH:

module testbench;

reg [7:0] A;

wire [2:0] Y;

wire valid;

priority\_encoder\_8 uut (.A(A), .Y(Y), .valid(valid));

initial begin

$monitor("A=%b -> Y=%b, Valid=%b", A, Y, valid);

A = 8'b00000000; #10;

A = 8'b00000001; #10;

A = 8'b10000000; #10;

A = 8'b01001000; #10;

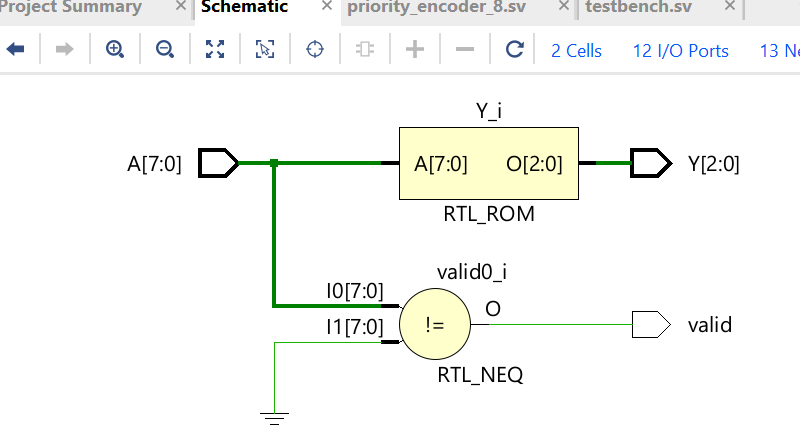
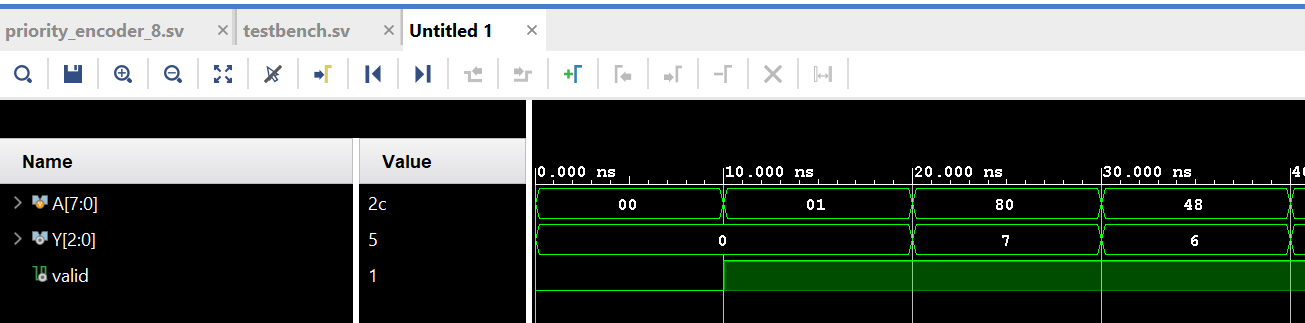
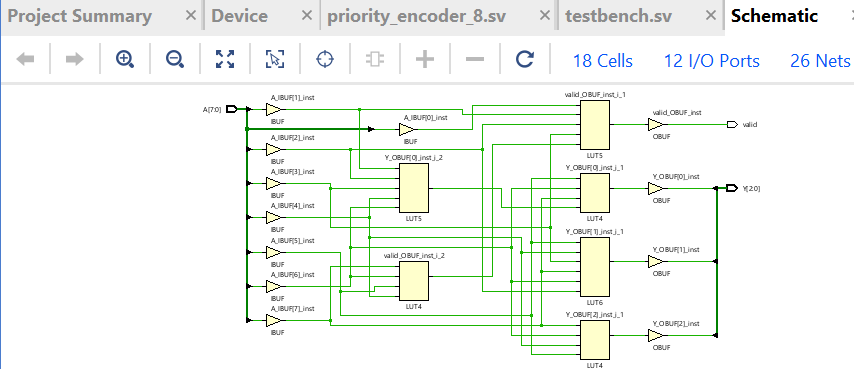
A = 8'b00101100; #10;

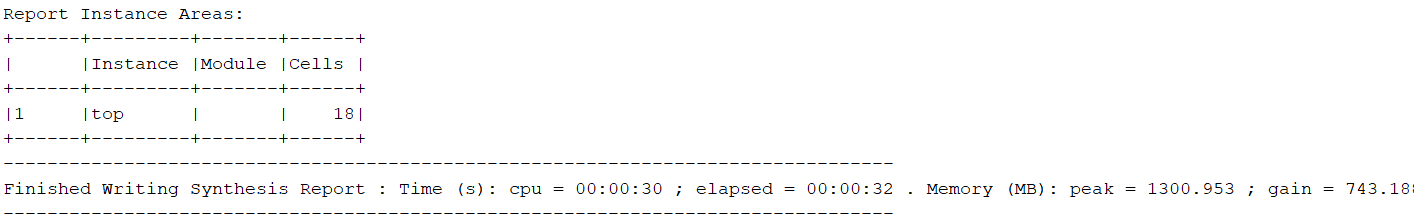
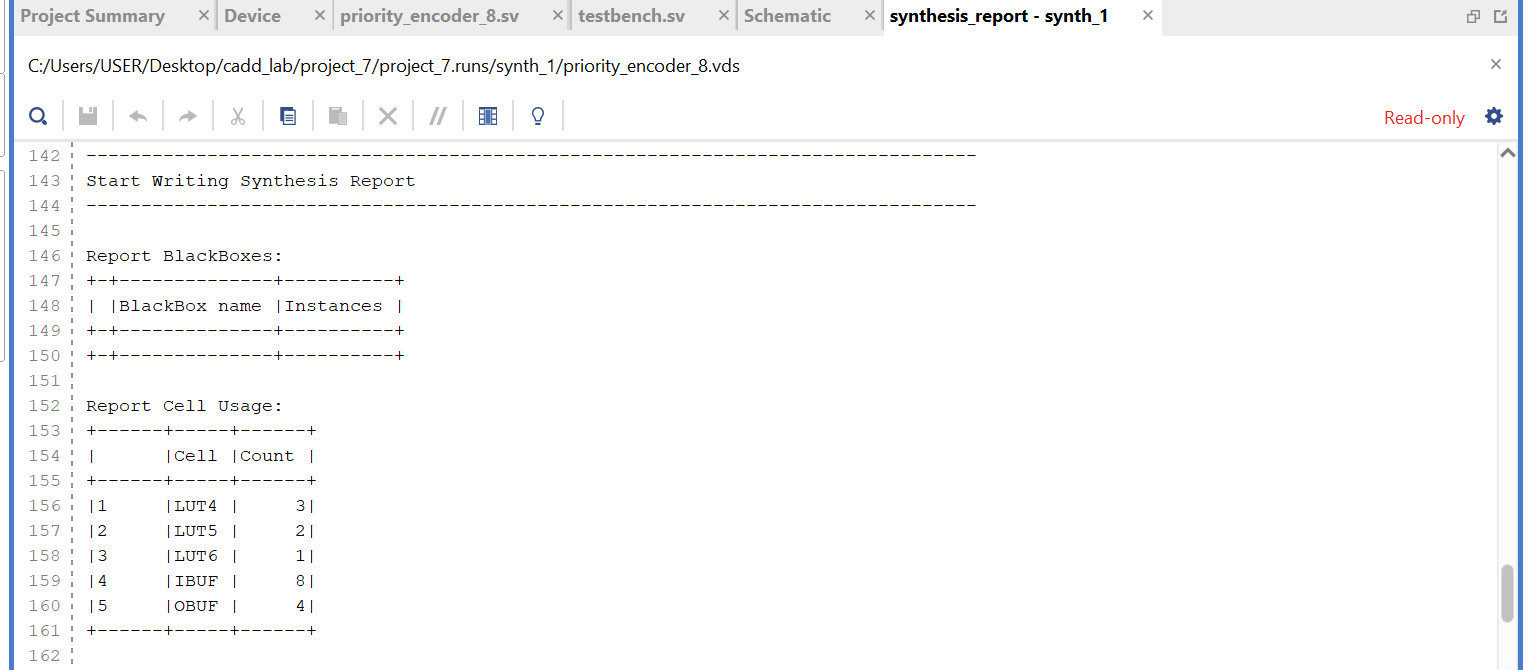
$finish;

end

endmodule

RTL:

WAVEFORM: TECHNOLOGY SCREESHOT

SYNTHESIS REPORT:

(i) FSM

Design code :

module fsm(input clk, reset, X, output logic [1:0] state);

parameter S0 = 2'b00, S1 = 2'b01, S2 = 2'b10;

always @(posedge clk or posedge reset) begin

if (reset)

state <= S0;

end

else begin

case (state)

S0: state <= X ? S1 : S0;

S1: state <= X ? S2 : S0;

S2: state <= X ? S2 : S1;

endcase

end

endmodule

TESTBENCH:

module testbench;

reg clk, reset, X;

wire [1:0] state;

fsm uut (.clk(clk), .reset(reset), .X(X), .state(state));

initial begin

clk = 0;

forever #5 clk = ~clk;

end

initial begin

$monitor("Time=%0t | Reset=%b, X=%b -> State=%b", $time, reset, X, state);

reset = 1; X = 0; #10;

reset = 0; X = 1; #10;

X = 1; #10;

X = 0; #10;

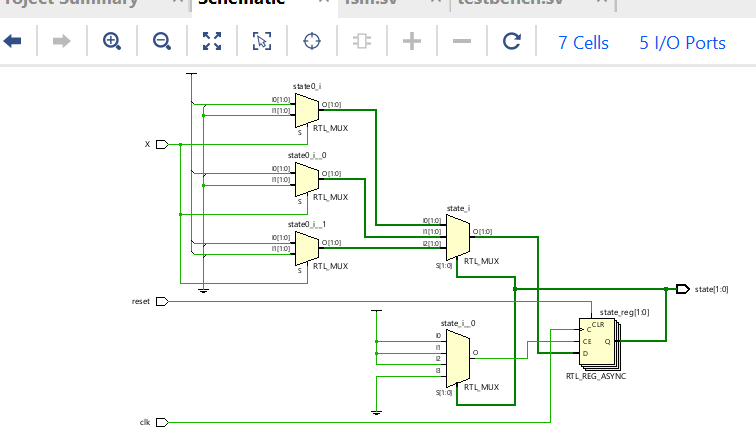
X = 0; #10;

$finish;

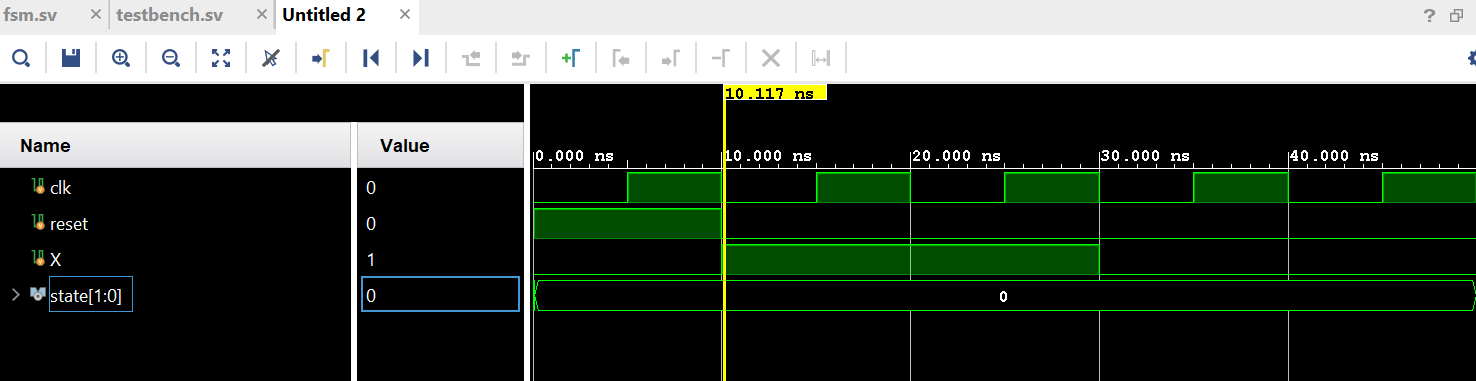
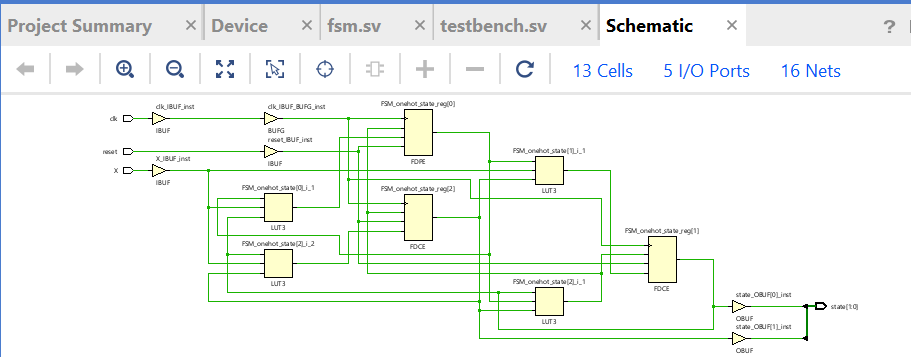
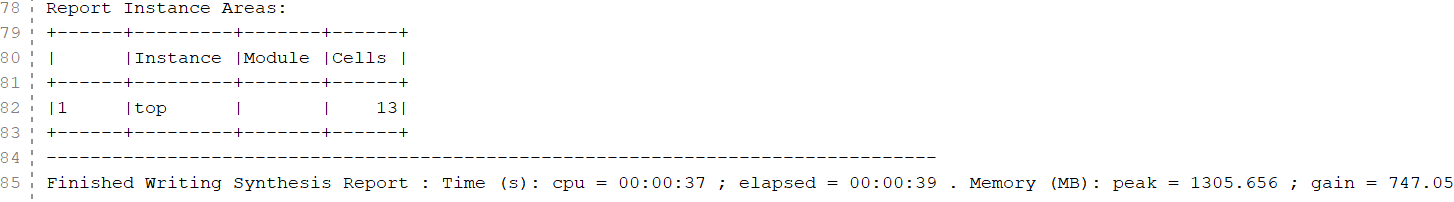
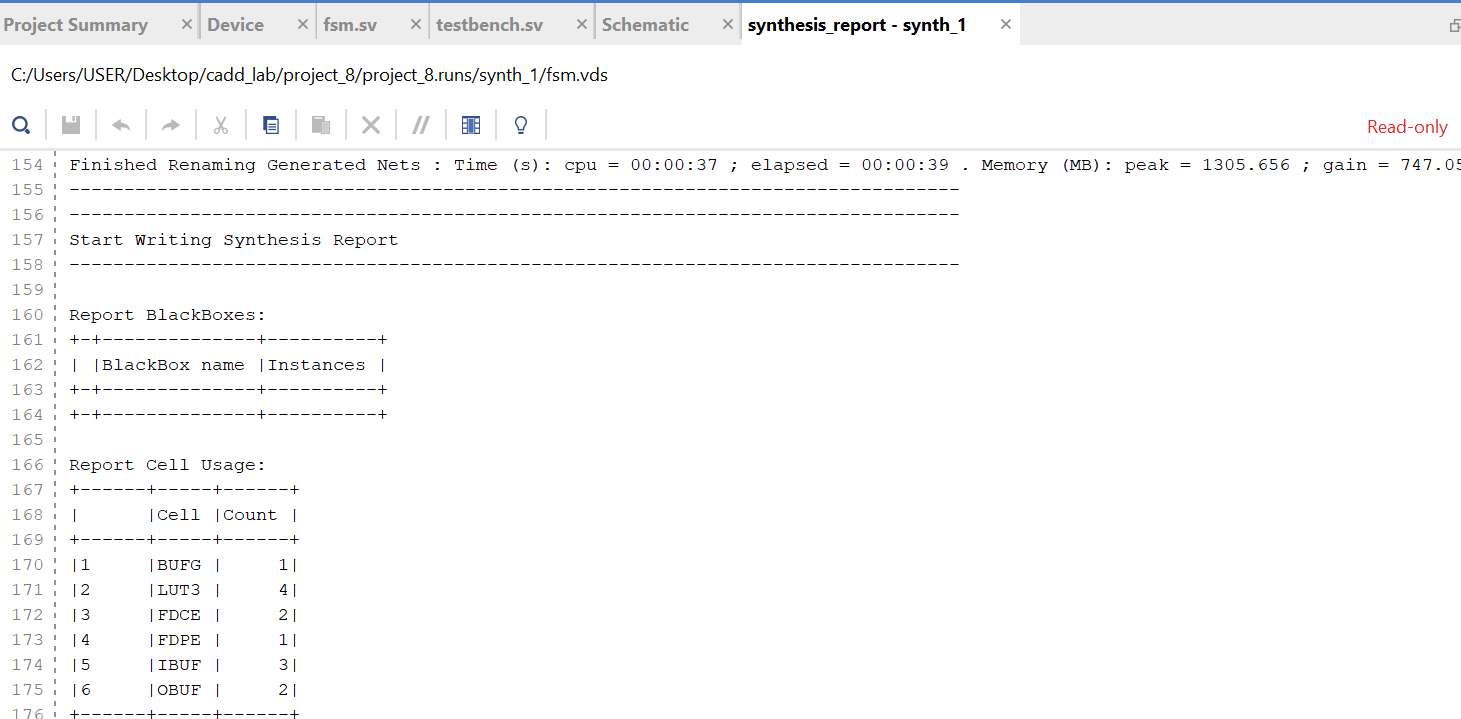
end

endmodule

RTL:



WAVEFORM:

TECHNOLOGY SCREENSHOT: SYNTHESIS REPORT:

(g) 3-to-8 Decoder

Design code;

module decoder\_3to8(input [2:0] A, output logic [7:0] Y);

always @(\*) begin

Y = 8'b00000000;

case (A)

3'b000: Y[0] = 1;

3'b001: Y[1] = 1;

3'b010: Y[2] = 1;

3'b011: Y[3] = 1;

3'b100: Y[4] = 1;

3'b101: Y[5] = 1;

3'b110: Y[6] = 1;

3'b111: Y[7] = 1;

endcase

end

endmodule

TESTBENCH:

module testbench;

reg [2:0] A;

wire [7:0] Y;

decoder\_3to8 uut (.A(A), .Y(Y));

initial begin

$monitor("A=%b -> Y=%b", A, Y);

A = 3'b000; #10;

A = 3'b001; #10;

A = 3'b010; #10;

A = 3'b100; #10;

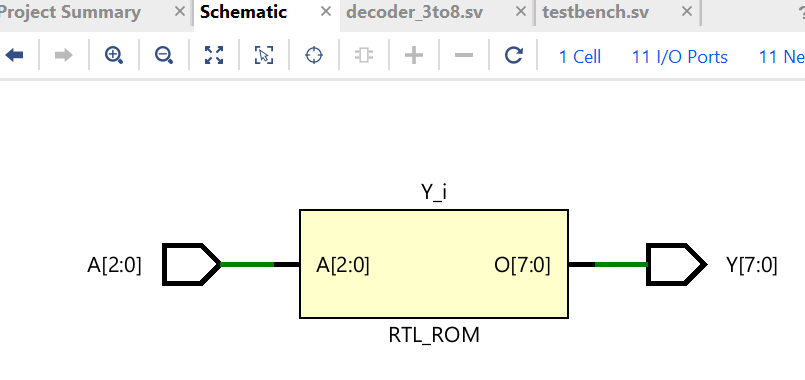
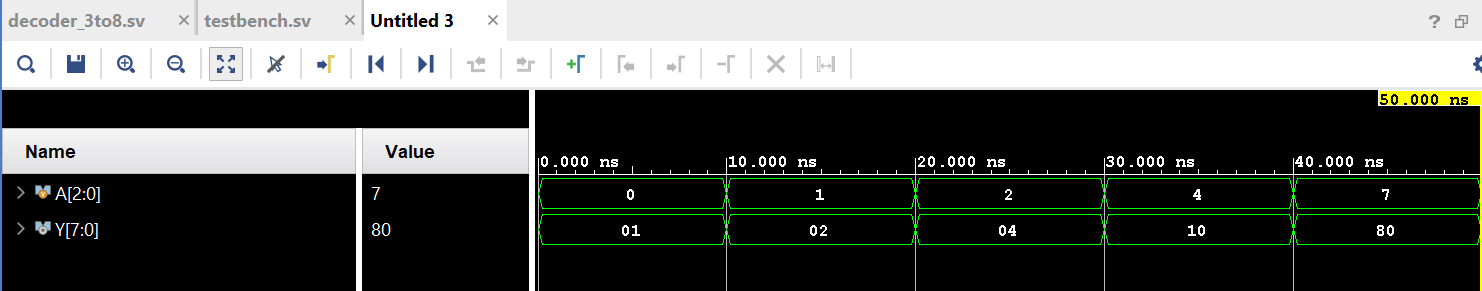
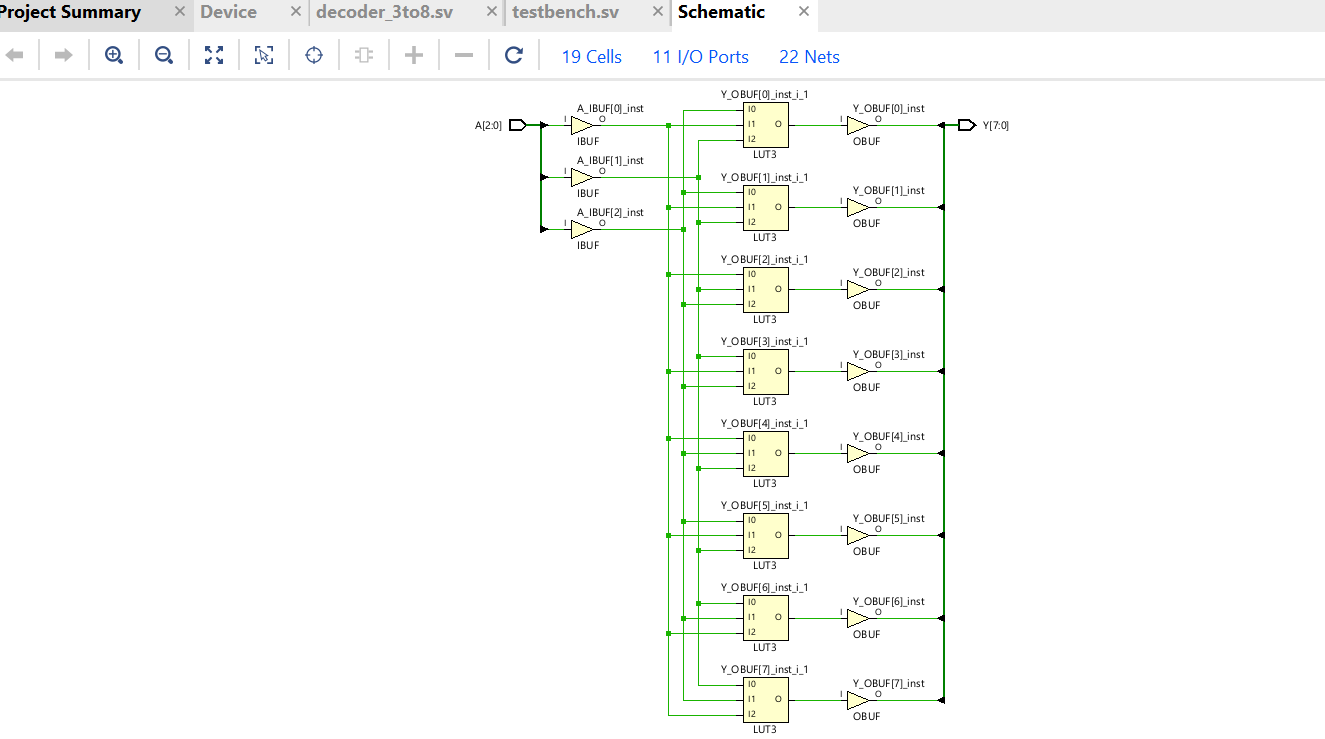
A = 3'b111; #10;

$finish;

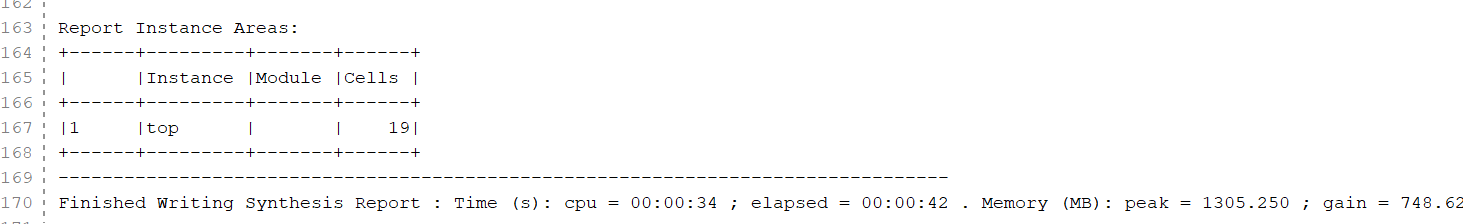
end

endmodule

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WAVEFORM:TECHNOLOGY SCREENSHOT:

SYNTHESIS REPORT:



(h) A 4-Bit carry propagate adder(with no carry in)

Design code

module carry\_propagate\_adder\_4bit\_no\_carry(input [3:0] A, B, output [3:0] Sum);

assign Sum = A + B;

endmodule

TESTBENCH:

module testbench;

reg [3:0] A, B;

wire [3:0] Sum;

carry\_propagate\_adder\_4bit\_no\_carry uut (.A(A), .B(B), .Sum(Sum));

initial begin

$monitor("A=%b (%d), B=%b (%d) -> Sum=%b (%d)", A, A, B, B, Sum, Sum);

A = 4'b0001; B = 4'b0010; #10;

A = 4'b0101; B = 4'b0011; #10;

A = 4'b1001; B = 4'b0110; #10;

A = 4'b1111; B = 4'b0001; #10;

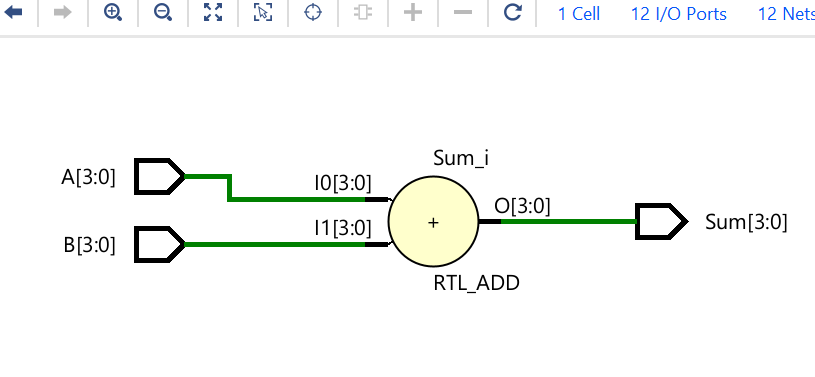
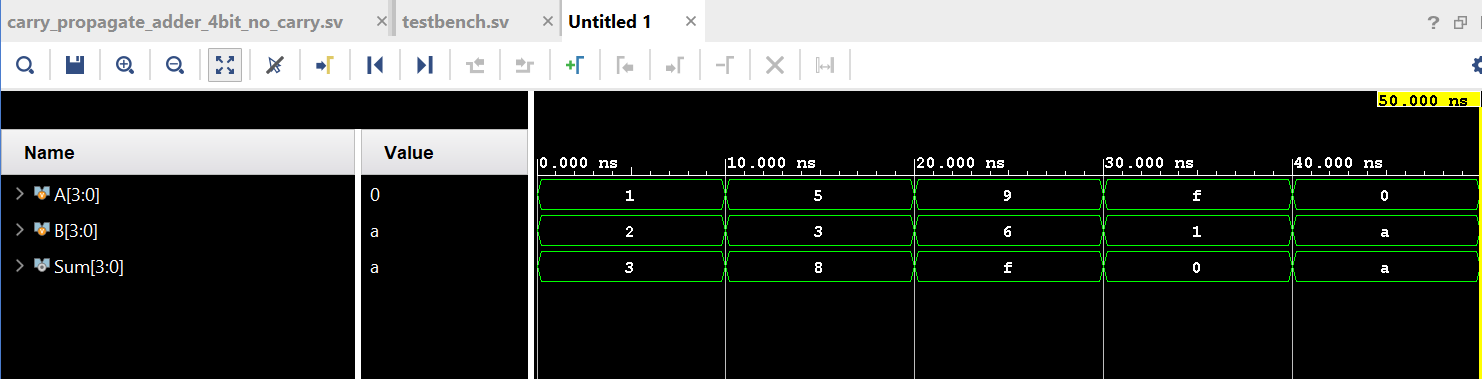
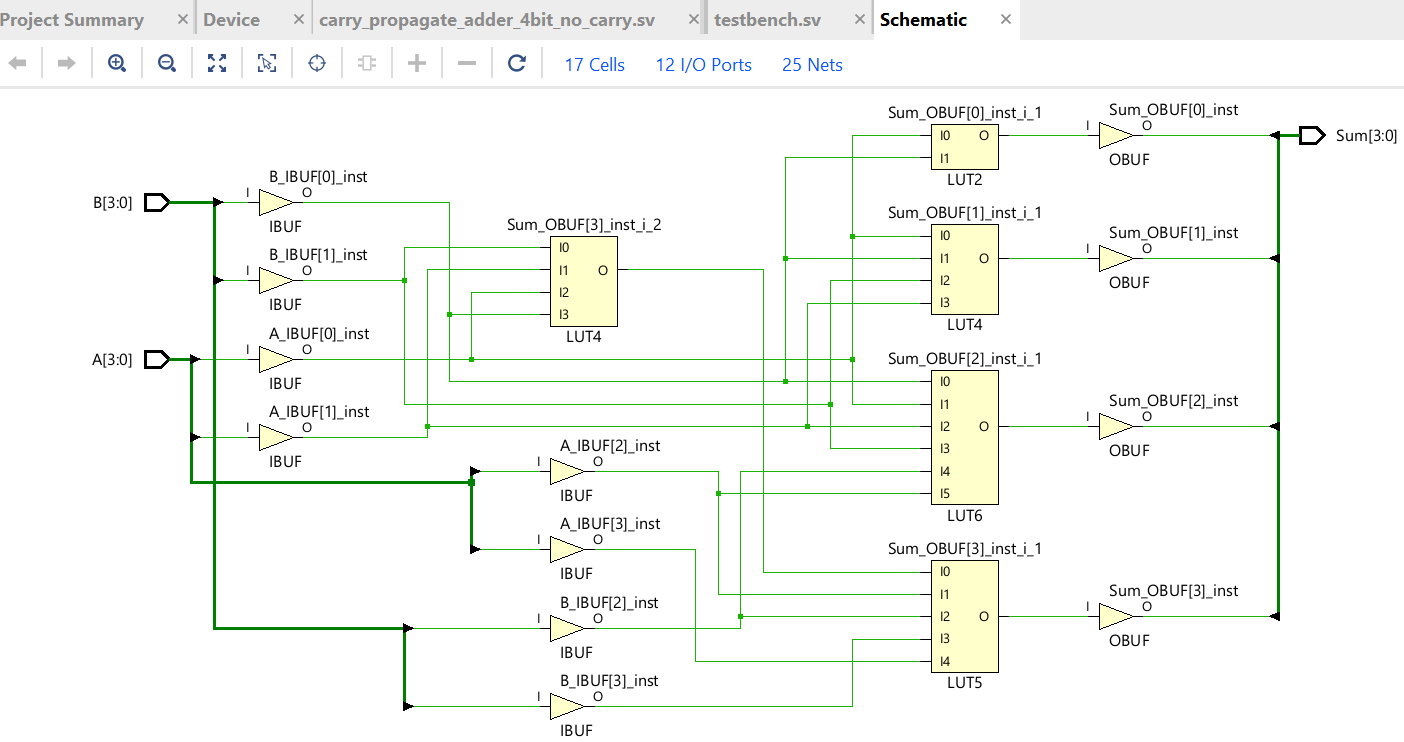
A = 4'b0000; B = 4'b1010; #10;

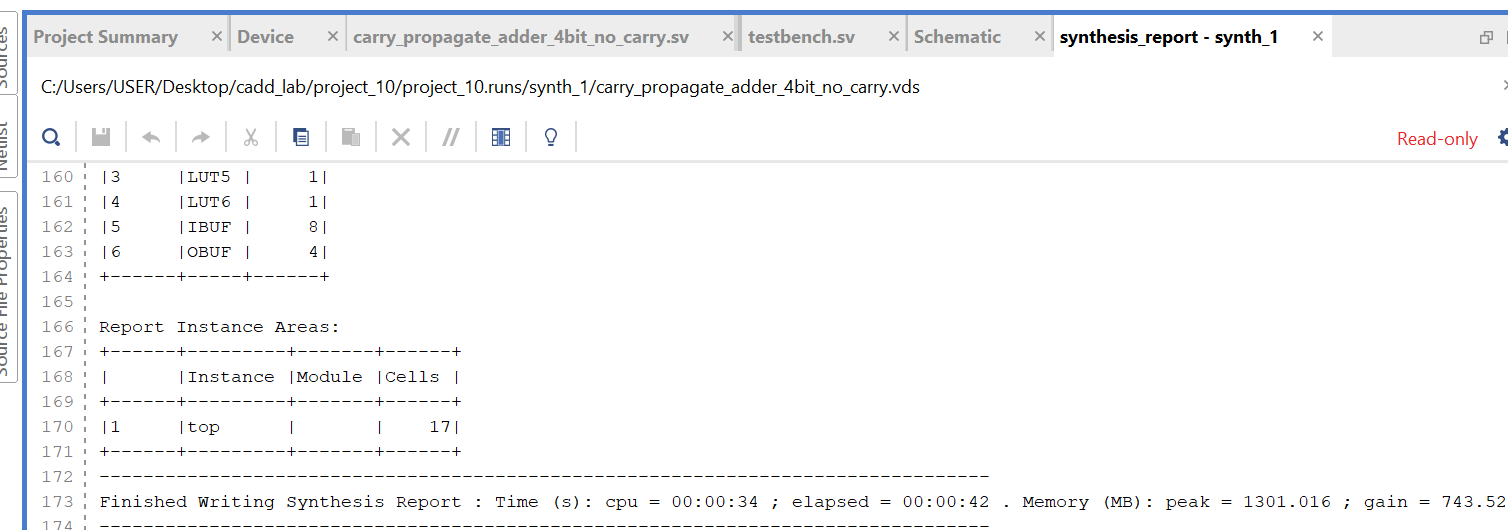
$finish;

end

endmodule

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WAVEFORM: TECHNOLOGY SCREENSHOT: 

SYNTHESIS REPORT: 

(j)The Gray code counter

DESIGN CODE:

module gray\_code\_counter (

input clk,

input reset,

output logic [2:0] gray\_code

);

logic [2:0] binary\_count;

always @(posedge clk or posedge reset) begin

if (reset) begin

binary\_count <= 3'b000;

end

else

begin

binary\_count <= binary\_count + 1;

end

end

always @(\*) begin

gray\_code = binary\_count ^ (binary\_count >> 1);

end

endmodule

TESTBENCH:

module testbench;

reg clk;

reg reset;

wire [2:0] gray\_code;

gray\_code\_counter uut (

.clk(clk),

.reset(reset),

.gray\_code(gray\_code)

);

always #5 clk = ~clk;

initial begin

clk = 0;

reset = 1;

#10;

reset = 0;

#100;

$stop;

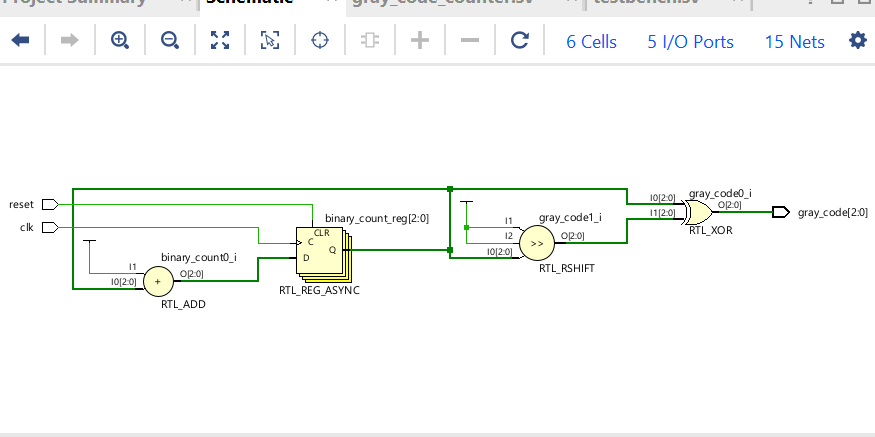
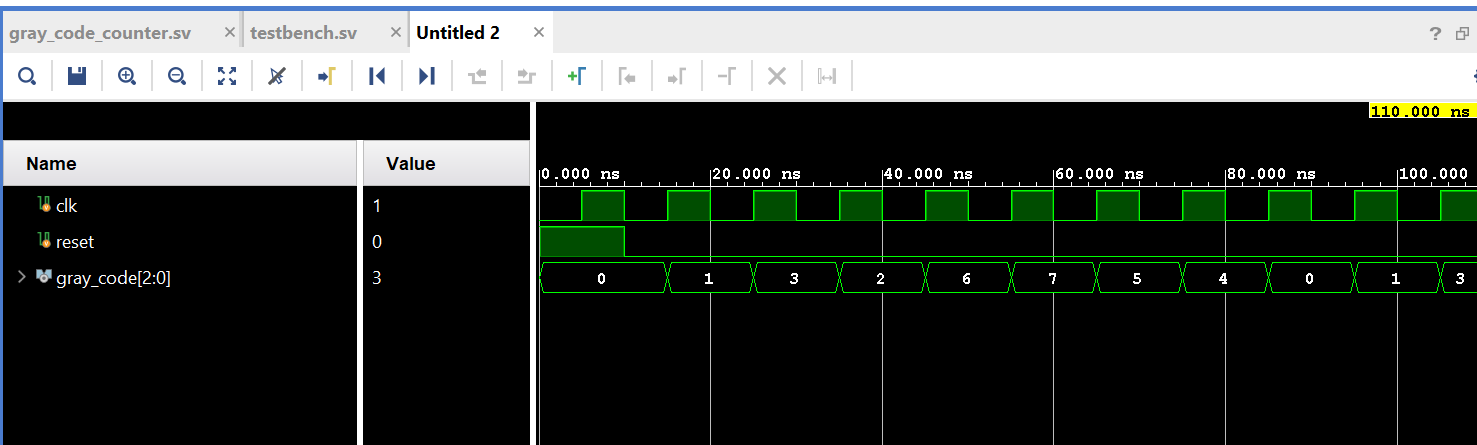
end

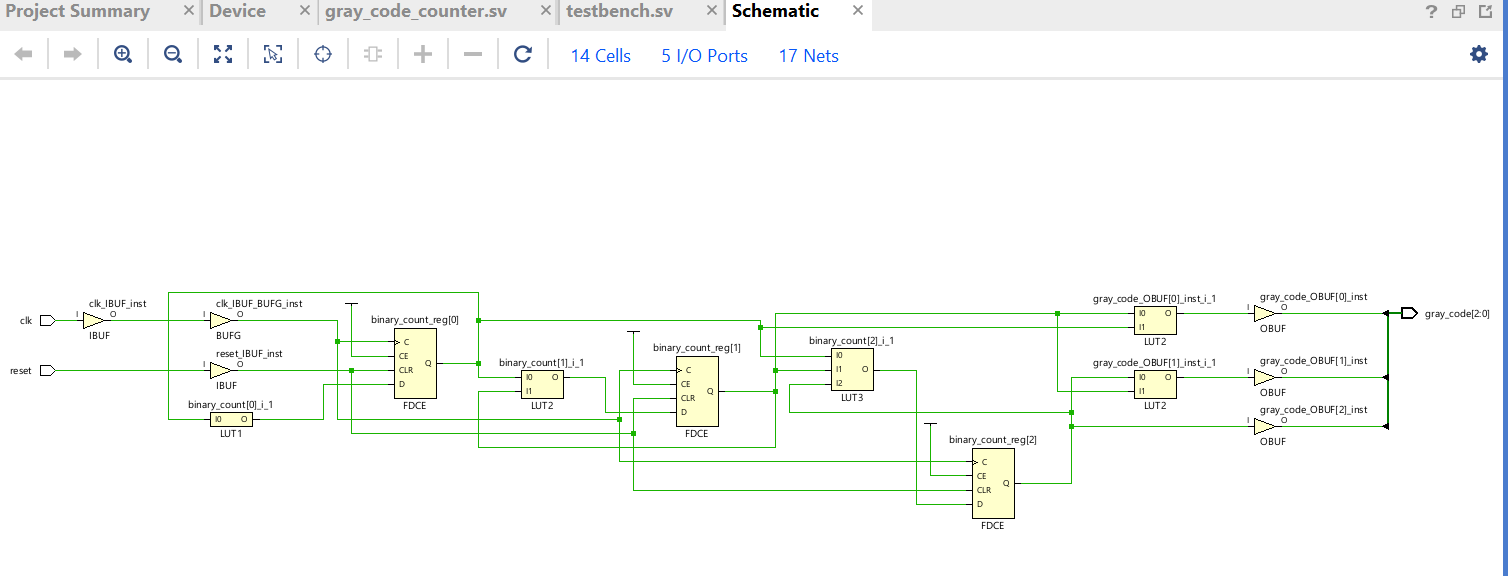
initial begin

$monitor("Time=%0t | Reset=%b | Gray Code=%b", $time, reset, gray\_code);

end

endmodule

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SYNTHESIS REPORT